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09/927,314	08/10/2001	Chris Macris		5545

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EXAMINER
PARSONS, THOMAS H

ART UNIT	PAPER NUMBER
1745	5

DATE MAILED: 06/25/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/927,314	MACRIS, CHRIS	
	Examiner	Art Unit	
	Thomas H Parsons	1745	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *10 August 2001* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-63* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *13-33 and 52-63* is/are allowed.

6)☒ Claim(s) *1,2,4-6,8-10,12 and 34-51* is/are rejected.

7)☒ Claim(s) *3,7 and 11* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *10 August 2001* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☒ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *4* .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Specification

1. The disclosure is objected to because of the following informalities:

Page 6:

Line 10, suggest deleting the second occurrence of "is"; and,

Page 11:

Line 7, suggest changing "48" to --46--.

Appropriate correction is required.

Drawings

2. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(5) because they do not include the following reference sign(s) mentioned in the description: "80" as mentioned on page 18, line 25; "82" as mentioned on page 18, lines 27 and 35, and on page 19, line 4; "84" as mentioned on page 18, line 34; "86" as mentioned on page 18, line 37; and "88" as mentioned on page 19, line 4.. A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

3. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(5) because they include the following reference sign(s) not mentioned in the description: "52a" as shown on Figure 5B; "96" and "98" as shown on Figures 12, 14 and 15; "100" as shown on Figure 13;

"102" as shown on Figure 14; and "104" as shown on Figure 15. A proposed drawing correction, corrected drawings, or amendment to the specification to add the reference sign(s) in the description, are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 1-2, 3-5, and 34-41 are rejected under 35 U.S.C. 103(a) as being unpatentable over Shiu et al. (5,956,569), and further in view of Assaderaghi et al. (6,121,661).

Claim 1: Shiu et al. in Figure 13A disclose a heat dissipating structure having including circuitry (20), and silicon substrate (10) wherein an electrical source is connected to the silicon Substrate (via bonding pads 24)(abs.; col. 2: 34-44; and col. 4: 7-50).

Shiu et al. do not disclose a silicon-on-insulator (SOI) structure having a buried oxide layer interposed between a silicon layer, including circuitry, and silicon substrate.

Assaderaghi et al. disclose on col. 1: 18-35 a silicon-on-insulator (SOI) structure having a buried oxide layer interposed between a silicon layer, including circuitry, and silicon substrate.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have modified the structure of Shiu et al. with the SOI structure of

Assaderaghi et al. because Assaderaghi et al. teach an SOI structure that would have provided an electrostatic discharge protection structure of SOI devices, and reduced parasitic capacitance thereby improving the performance of reliability of SOI devices.

As to the recitation, "whereby the charge carrier flow travels in a direction from the hot region on the SOI structure outward toward the perimeter of the silicon substrate", it would have been obvious to one of ordinary skill in the art at the time the invention was made to have expected the claimed charge carrier flow as the structure of the Shiu et al. combination is structurally similar to that instantly claimed.

Claim 2: Shiu et al. in Figure 13A disclose at least a portion of the silicon substrate is doped to yield an N-type region (46n) (col. 3: 13-36).

Claim 4: Shiu et al. in Figures 15A and 16A disclose that the silicon substrate is electrically in series with an electrical load (e.g. a laser) other than itself (col. 1: 14-16).

Claim 5: Shiu et al. in Figure 13A disclose a silicon substrate (10)(col. 4: 15-19). The recitation "is utilized as a resistive load for an electronic component" has been construed as a statement of intended use which does not alter the overall physical structure of the device, and, therefore, has been given little patentable weight. However, because the device of the Shiu et al. combination is structurally similar to that instantly claimed, it appears capable of being utilized as claimed.

Claim 34: Shiu et al. in Figure 13A disclose a method of manufacturing a heat dissipating structure, the structure comprising silicon substrate (10), more than one thermoelement couple, each with at least one heat absorbing (i.e. junctions positioned immediate IC 20) and one heat rejecting junction (i.e. junctions positioned immediate the heat

sink) and P-type (46p) and negative-type N-type (46n) conductivity dopants comprising: (a) Selectively depositing the P and N-type dopants into at least one face of the substrate to form a pattern of P and N-type conductivity thermoelements within the silicon substrate; (b) Electrically bonding the P and N-type conductivity thermoelements at heat absorbing and heat rejecting junctions to form thermoelement couples (col. 3: 5-24; and col. 5: 36-col. 6: 26).

Shiu et al. do not disclose a silicon-on-insulator (SOI) structure having a buried oxide layer interposed between a silicon layer and a silicon substrate.

Assaderaghi et al. disclose on col. 1: 18-35 a silicon-on-insulator (SOI) structure having a buried oxide layer interposed between a silicon layer and a silicon substrate.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have modified the structure of Shiu et al. with the SOI structure of Assaderaghi et al. because Assaderaghi et al. teach an SOI structure that would have provided an electrostatic discharge protection structure of SOI devices, and reduced parasitic capacitance thereby improving the performance of reliability of SOI devices.

Claim 35: Shiu et al. in Figure 13A disclose heat absorbing junctions (i.e. junctions positioned immediate IC 20) positioned near the center of the SOI substrate and the heat rejecting junctions (i.e. junctions positioned immediate the heat sink) positioned near the perimeter of the substrate (Col. 4: 7-35).

Claim 36: Shiu et al. on col. 5: 12-35 disclose that a dielectric, such as oxide or nitride, is added to the physical regions (42, 34) between each P and N-type thermoelement in order to provide electrical insulation between each thermoelement.

Claim 37: Shiu et al. in Figure 13 A disclose physical regions (holes 28 and 32) between each P and N-type thermoelement are removed in order to provide electrical insulation between each thermoelement (col. 2: 58-64).

Claim 38: Shiu et al. on col. 2: 34-44 disclose applying a voltage to at least one thermoelement couple (via bonding pads 24).

Claim 39: Shiu et al. in Figures 15A and 16A disclose that the thermoelement couple is electrically in series with an electrical load (module 74) other than itself (col. 1: 14-16 which discloses a laser).

Claim 40: Shiu et al. in Figure 13A disclose a thermoelement couple (i.e. the bond between the n- and p-type material). The recitation "is utilized as a resistive load for an electronic component" has been construed as a statement of intended use which does not alter the overall physical structure of the device, and, therefore, has been given little patentable weight. However, because the device of the Shiu et al. combination is structurally similar to that instantly claimed, it appears capable of being utilized as claimed.

Claim 41: The recitation "wherein a voltage and current is generated by at least one thermoelement couple and is consumed by an external electric load" has been construed as a process limitation which does not alter the overall physical structure of the device, and therefore, has been given little patentable weight. However, because the structure of the Shiu et al. combination is structurally similar to that instantly claimed, it appears capable of functioning as claimed.

6. Claims 6, 9-10 and 12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Burward-Hoy (5,637,921), and further in view of Marmillion et al. (6,242,778).

Claim 6: Burward-Hoy in Figure 2 discloses a heat dissipating having a substrate, the structure comprising: at least one electrically conductive member (201) attachable to the substrate (IC chip 235); and an electrical source (265, 275) connected to the electrically conductive member (col. 2: 49-col. 3: 40).

Burward-Hoy does not disclose a silicon-on-insulator structure having a buried oxide layer interposed between a silicon layer and silicon substrate.

Marmillion et al. disclose a silicon-on-insulator structure having a buried oxide layer interposed between a silicon layer and silicon substrate (abs.; and col. 1: 11-25).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have substituted the substrate of Burward-Hoy with the SOI structure of Marmillion et al. because Marmillion et al. teach an SOI structure that would have provided an SOI with thermal conductors in the insulating layer of the SOI wherein the conductors are capable of receiving a heat sink for cooling semiconductor chips near device junctions thereby improving the overall efficiency of the conductive member.

As to the recitation, "whereby the charge carrier flow travels in a direction from the hot region on the SOI structure outward toward the perimeter of the silicon substrate", it would have been obvious to one of ordinary skill in the art at the time the invention was made to have expected the claimed charge carrier flow as the structure of the Burward-Hoy combination is structurally similar to that instantly claimed.

Claim 9: The rejection is as set forth above in claim 1 wherein Burward-Hoy discloses an electrically conductive member. The recitation "is utilized as a resistive load for an electronic component" has been construed as a statement of intended use which does not alter the overall physical structure of the device, and, therefore, has been given little patentable weight.

However, because the device of the Shiu et al. combination. Is structurally similar to that instantly claimed, it appears capable of being utilized as claimed.

Claim 10: Burward-Hoy in Figure 2 discloses a package (as defined by 202, 205 and 212) for housing the silicon substrate (col. 2: 49-col. 3: 54).

Claim 12: Burward-Hoy in Figure 2 discloses that the SOI structure attachment (electrically conductive copper 230) to the electrically conductive member is electrically conductive (col. 3: 29-32).

7. Claim 8 is rejected under 35 U.S.C. 103(a) as being unpatentable over Burward-Hoy, and further in view of Marmillion et al as applied to claim 6 above, and further in view of Bhatia (6,094,919).

Burward-Hoy and Marmillion et al. are as applied, argued and disclosed above, and incorporated herein.

The Burward-Hoy combination does not disclose that the electrically conductive member is electrically in series with an electrical load other than itself.

Bhatia in Figure 2 discloses that the electrically conductive member (35) is electrically in series with an electrical load (circuit board 40) other than itself.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have modified the apparatus of the Burward-Hoy combination with the load of Bhatia because teaches that it would have been known to apply an electrically conductive member in series with an electrical load to provide for operating an IC device at significantly reduced temperatures thereby resulting in more efficient heat dissipation and lower operating cost.

8. Claims 42-51 are rejected under 35 U.S.C. 103(a) as being unpatentable over Buist (5,022,928), and further in view of Marmillion et al.

Claim 42: Buist in Figure 2 discloses a heat dissipating, the structure comprising semiconductor substrate, more than one thermoelement couple stage (stages 1, 2, 3), each stage containing at least one thermoelement couple (col. 3: 8-13), each with at least one heat absorbing (hot core) and heat rejecting (cold core) junction, wherein all thermoelement couple stages are fabricated within at least one silicon substrate (col. 2: 56-col. 4: 19).

Buist does not disclose a silicon-on-insulator structure having a buried oxide layer interposed between a silicon layer and silicon substrate.

Marmillion et al. disclose a silicon-on-insulator structure having a buried oxide layer interposed between a silicon layer and silicon substrate (abs.; and col. 1: 11-25).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have substituted the substrate of Buist with the SOI structure of Marmillion et al. because Marmillion et al. teach a known SOI structure that would have provided an SOI with thermal conductors in the insulating layer of the SOI wherein the

conductors are capable of receiving a heat sink for cooling semiconductor chips near device junctions thereby improving the overall efficiency of the conductive member.

Claim 43: Buist on col. 2: 56-col. 3: 44; and col. 3:53-col. 4: 19 discloses each successive thermoelement couple

stage laterally displaced from the previous stage and the heat source.

Claim 44: Buist discloses each stage positioned outside the entire perimeter of the previous stage and each successive stage (Figure 2 shows stage 2 outside the perimeter of stage 1, and stage 3 is outside the perimeter of stage 22) (col. 2: 56-col. 4: 19).

Claim 45: Buist on col. 3: 53-63 discloses each heat absorbing junction positioned near the center of each thermoelement couple stage and heat rejecting junction is positioned near the perimeter of each stage.

Claim 46: Buist on col. 3:45-56 discloses a dielectric added to the physical regions between each thermoelement stage in order to provide electrical insulation between each thermoelement.

Because the claim has been given its broadest interpretation, the narrow limitation "such as oxide or nitride" has not been considered. However, it the Applicant wishes for the narrower limitation to be considered, the Examiner suggests providing this limitation as a separate claim.

Claim 47: Buist on col. 2: 9-22 discloses a voltage applied to at least one thermoelement couple.

Claim 48: Buist on col. 3: 48-52 discloses the thermoelement couple electrically in series with an electrical load (i.e. hot spot forming device) other than itself.

Claim 49: Buist on col. 2: 9-col. 3: 44 discloses a thermoelement couple. The recitation "is utilized as a resistive load for an electronic component" has been construed as a statement of intended use which does not alter the overall physical structure of the device, and, therefore, has been given little patentable weight.

However, because the device of the Buist combination is structurally similar to that instantly claimed, it appears capable of being utilized as claimed.

Claim 50: The recitation "wherein a voltage and current is generated by at least one thermoelement couple and is consumed by an external electric load" has been construed as a process limitation which does not alter the overall physical structure of the device, and therefore, has been given little patentable weight. However, because the structure of the Buist. combination is structurally similar to that instantly claimed, it appears capable of functioning as claimed.

Claim 51: Buist on col. 2: 9-col. 3: 44 discloses each dissimilar thermoelement, comprising each thermoelement couple, electrically bonded to each other at both the heat absorbing and heat rejecting junctions thereby creating closed
electrical circuit thermoelement couples.

Allowable Subject Matter

9. Claims 13-33 and 52-63 are allowable over the prior art of record.

10. Claims 3, 7 and 11 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Reasons for Indicating Allowable Subject Matter

11. The following is a statement of reasons for the indication of allowable subject matter:

The prior art of record teaches attaching a silicon substrate to a heat sink/spreader structure wherein a thermoelement couple is created through the bonding between dissimilar semiconductors (n- and p-type) comprising the heat sink/spreader structure.

In contrast, the claimed invention requires creating a thermoelement couple through the bonding between the silicon substrate and a dissimilar conductor or semiconductor.

Therefore, a search of the prior art of record failed to reveal or explicitly teach, alone or in combination, what is instantly claimed: in particular.

A heat dissipating silicon-on-insulator structure having a buried oxide layer interposed between a silicon layer and silicon substrate, said substrate comprising: at least one thermoelement couple, said couple comprised of the silicon substrate and at least one dissimilar conductor electrically bonded to the silicon substrate thereby creating junctions; and said thermoelement couple comprises at least one heat absorbing junction and at least one heat rejecting junction wherein the heat absorbing junction is positioned near the center of the SOI substrate and the heat rejecting junction is positioned near the perimeter of the substrate. For this reason, claim 13 and claims 14-21, which are dependent thereon, are patentably distinct from the prior art of record.

A heat dissipating silicon-on-insulator structure, the structure comprising an SOI structure consisting of a buried oxide layer interposed between a silicon layer and silicon substrate, the silicon substrate attachable to a heat sink/spreader structure comprising: a heat sink/spreader structure wherein at least one thermoelement couple is created through the bonding between at least one semiconductor to at least one dissimilar conductor; and the dissimilar conductor comprises at least one heat absorbing junction and at least one heat rejecting junction. For this reason, claim 22 and claims 23-33, which are dependent thereon, are patentably distinct from the prior art of record.

A method of manufacturing a heat dissipating silicon-on-insulator wafer, the wafer includes a top silicon wafer and bottom silicon wafer wherein the bottom wafer comprises at least one thermoelement couple, the couple includes at least two dissimilar thermoelements with at least one heat absorbing and more one heat rejecting junction comprising the steps of: (a) Applying an oxide layer between the top silicon wafer and the bottom silicon wafer; (b) Wafer bonding the top silicon wafer to the bottom silicon wafer via the oxide layer. For this reason, claim 52 and claims 53-63, which are dependent thereon, are patentably distinct from the prior art of record.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thomas H Parsons whose telephone number is (703) 306-9072. The examiner can normally be reached on M-F (7:00-4:30) First Friday Off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Pat Ryan can be reached on (703) 308-2383. The fax phone numbers for the

organization where this application or proceeding is assigned are (703) 872-9310 for regular communications and (703) 872-9311 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0661.

Thomas H Parsons
Examiner
Art Unit 1745

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June 17, 2003

Patrick Ryan
Supervisory Patent Examiner
Technology Center 1700